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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,141	04/01/2004	Heung-Lyul Cho	0630-1979P	6546

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EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	PAPER NUMBER
2871	

NOTIFICATION DATE	DELIVERY MODE
06/03/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/814,141	CHO ET AL.	
	Examiner	Art Unit	
	ANDREW SCHECHTER	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,15,16,20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *20,23 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11 March 2009 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The applicant argues [pp. 8-9] that the cited references fail to teach or suggest the features of amended independent claim 1, and quotes 17 lines of the claim, but does not specifically compare any limitations of the claim to the prior art as applied in the previous rejections. To the examiner, it appears that the amended claim should be rejected based on the same prior art as applied before, though the wording of the rejection has to be modified due to the amendments to the claims. To the extent that this is a new grounds of rejection, it is necessitated by the applicant's amendment.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "the source/drain electrode" in line 27 should be "the source and drain electrodes". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Deane et al.,* U.S. Patent No. 6,686,229 in view of official notice / admitted prior art, in view of *Chae*, US 2002/0135710, and further in view of *Baughman et al.,* U.S. Patent No. 5,441,593.

Deane discloses [see Fig. 1, for instance] a fabrication method of a liquid crystal display device, comprising: providing a substrate [1], forming a gate line [5] on the substrate by applying a gate photoresist pattern by printing [col. 7, lines 60-67], sequentially forming a gate insulating layer [13], a semiconductor layer [17], and a high-concentrated N+ layer [19] over the gate line; forming an active region including the high-concentrated N+ layer by applying an active photoresist pattern by printing [col. 7, lines 60-67], wherein the active region is formed by sequentially removing the high-concentrated N+ layer and the semiconductor layer using the active photoresist pattern formed by printing as a mask [see Fig. 1b]; removing the active resist pattern [inherent]; forming a conductive layer [23] over the active region and the gate insulating layer; forming source and drain electrodes [29, 27]; forming a passivation layer [33] over the source and drain electrodes; forming a contact hole photoresist pattern [34] over the passivation layer by printing process [col. 6, lines 17-22], removing the passivation layer by using the contact hole photoresist pattern as a mask to form a contact hole [35], removing the contact hole photoresist pattern [inherent]; forming a pixel electrode layer over the passivation layer and the contact hole, forming a pixel electrode photoresist

pattern [col. 7, lines 60-67] over the pixel layer by a printing process, and removing the pixel electrode layer by using the pixel electrode photoresist pattern as a mask to form a pixel electrode [37].

For the steps of forming the gate line, forming the semiconductor layer and N+ layer, and forming the pixel electrode, the reference describes directly printing the layers onto the substrate [as can be seen from the "tails" shown in the figures, for instance]. However, the reference also explicitly states [col. 7, lines 60-67] that these printing processes can be replaced with the process of covering the substrate with the material of the layer, printing a photoresist pattern onto the material, and etching to pattern the layer. The reference also provides motivation to do so, in that it avoids the need to use conventional photolithography to process the photoresists, thus lowering costs while not needing to directly print the layer. The examiner has therefore treated the relevant claim limitations as explicitly disclosed by the reference, as noted above; alternatively, they could be considered as not disclosed by the particular embodiment of Fig. 1 (and initial discussion thereof), but obvious to one of ordinary skill in the art at the time of the invention due to these teachings of *Deane* [col. 7, lines 60-67]. In either case, these claim limitations are met by *Deane*.

Deane does not explicitly disclose depositing a photoresist layer over the conductive layer, applying a mask over the photoresist layer, and performing a lithography process, to form a photoresist pattern, and removing the conductive layer by using the photoresist layer pattern as a mask to form the source and drain electrodes. Instead, *Deane* merely states that the conductive layer is "then patterned using

conventional photolithography" [col. 5, lines 35-36]. The examiner takes official notice that it was well-known in the art for conventional photolithography to include steps of depositing a photoresist layer over a conductive layer, applying a mask over the photoresist layer, and performing a lithography process to form a photoresist layer pattern [this taking of official notice was not traversed by the applicant, therefore the statement is considered admitted prior art, see MPEP 2144.04], and then using this photoresist layer pattern as a mask to form the source and drain electrodes. It would have been obvious to one of ordinary skill in the art at the time of the invention to have these steps in the method of *Deane*, motivated by the desire to use conventional photolithographic techniques, having high reliability and precision, to form the source and drain electrodes.

Deane does not disclose removing the high-concentrated N+ layer above a channel region by using the photoresist layer pattern as a mask. Instead, the photoresist layer pattern is used as a mask to remove the conductive layer to form a source and drain electrodes and the photoresist layer pattern is then removed; the source and drain electrodes themselves (instead of the identically shaped photoresist layer pattern) are then used as the mask to remove the high-concentrated layer above the channel region.

Chae discloses [see Fig. 6C, paragraph 0061, for instance] a method of forming an analogous TFT, in which the source and drain electrodes [35, 37] are formed, the photoresist is removed, and the source and drain electrodes are then used as the mask to remove the high-concentrated layer [47], just as in *Deane*. *Chae* then goes on to say

[paragraph 0062] that alternatively the photoresist can be left in place and used as the mask in removing the high-concentrated layer, just as in the present application. This is evidence that the two sequences are considered art-recognized equivalents. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the photoresist as the mask for removing the high-concentrated layer, and only then removing the photoresist layer pattern, motivated by the art-recognized equivalence of the two methods.

Regarding the limitations amended to claim 1 in the response of 11 August 2008, namely that the relevant printing processes use a thermal transfer injection nozzle, including a resist storing layer for storing an injected resist, a thin film resistor for heating a thin-deposited resist electrically, a vapor heated by the thin film resistor, and an injection hole plate including an injection hole that injects a resist. Previously the examiner had taken official notice that inkjet printing was known in the art, and as this had not been traversed by the applicant, this was taken as admitted prior art [see MPEP 2144.04]; the use of inkjet printing was held to have been obvious to one of ordinary skill in the art at the time of the invention in this case in *Deane,* motivated by its being a reliable, cost-effective technique for printing. This remains valid. However, the taking of official notice did not extend to the amended details of the inkjet process.

Baughman discloses [see Fig. 1 and compare with the applicant's Fig. 2] such a thermal transfer injection nozzle, with resist storing layer [17], thin film resistor [16], vapor [col. 1, lines 35-37, for instance], and injection hole plate [22] including an injection hole [20] as recited. It would have been obvious to one of ordinary skill in the

art at the time of the invention to use such a thermal transfer injection nozzle for the relevant printing processes, motivated by *Baughman's* teaching that such an injection nozzle can be manufactured precisely and can achieve uniform controlled printing of material from multiple nozzles, thus producing the desired printed patterns on the substrate.

Claim 1 is therefore unpatentable.

Since the other steps are done by printing rather than conventional photolithography, the mask applied over the photoresist layer in the step of applying the mask is the only mask applied throughout the method of the independent claim, so claim 15 is also unpatentable. The printing is ink jet printing, so claim 16 is also unpatentable.

Election/Restrictions

5. Claims 20, 23, and 24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 6 January 2006.

Claims 20 and 24 have been amended to recite limitations related to forming a stepped active photoresist pattern and ashing, so the claims are drawn to the embodiment of Fig. 5, the non-elected species IB. Claim 23 depends from claim 20.

6. This application contains claims 20, 23, and 24 drawn to an invention nonelected with traverse in the filing of 6 January 2006. A complete reply to the final rejection must

include cancellation of nonelected claims or other appropriate action (37 CFR 1.144). See MPEP § 821.01.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 2001/0040648 to *Ono et al.* discloses [see Fig. 7, for instance] a method of exposing a part of the active photoresist pattern on a channel region by using a mask for controlling an optical amount and removing the exposed active photoresist pattern on a channel region to form a stepped active photoresist pattern, wherein a degree of the removed active photoresist pattern is different at time of development according to a degree of exposure of light, patterning the conductive layer, impurity-doped layer, and semiconductor layer by using the stepped active photoresist pattern as a mask, ashing a part of the stepped active photoresist pattern to remove the photoresist pattern on the channel region, and removing the conductive layer and the impurity-doped layer on the channel region to form source and drain electrode electrically separated from each other.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
Technology Center 2800
28 May 2009